IN THE CLAIMS

1. (Cancelled)

2. (Currently Amended) A semiconductor memory device comprising:

a voltage level detector configured to sense a voltage and configured to generate a power-up signal while the voltage is less than a minimum voltage required to operate the device;

a command register configured to generate a command busy signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal and the command busy signal; and

a ready/busy driver configured to drive a ready/busy signal in response ~~that is responsive~~ to the busy enable signal~~; and~~.

~~a command register coupled to an input of the ready/busy driver controller.~~

3. (Previously presented) The semiconductor memory device of claim 2, wherein the command register comprises:

a program command register configured to provide a program busy signal to the ready/busy driver controller; and

an erase command register configured to provide an erase busy signal to the ready/busy driver controller.

4. (Previously presented) The semiconductor memory device of claim 3, wherein the program busy signal indicates that the memory device is in a program mode.

5. (Previously presented) The semiconductor memory device of claim 3, wherein the erase busy signal indicates that the memory device is in an erase mode.

6. (Currently Amended) The semiconductor memory device of claim ~~1~~2, wherein the ready/busy driver controller comprises:

a control signal generator configured to generate a first and a second control signal in response to the power-up signal; and

a level shifter configured to generate the busy enable signal in response to the first and second control signals.

7. (Currently Amended) The semiconductor memory device of claim ~~1~~2, wherein the ready/busy driver comprises:

a ready/busy pin;

an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal; and

a pull up load connected to the ready/busy pin.

8. (Previously presented) The semiconductor memory device of claim 7, wherein the memory device is in a busy state during a power-up period when the voltage at the ready/busy pin is at a low state.

9. (Previously presented) The semiconductor memory device of claim 8, wherein the memory device is in a ready state after the power-up period.

10. (Cancelled)

11. (Previously presented) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal; and

a ready/busy driver that is responsive to the busy enable signal;

wherein the ready/busy driver controller comprises:

a control signal generator configured to generate a first and a second control signal in response to the power-up signal; and

a level shifter configured to generate the busy enable signal in response to the first and second control signals.

12. (Previously presented) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal; and

a ready/busy driver that is responsive to the busy enable signal;

wherein the ready/busy driver controller comprises:

a ready/busy pin;

an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal; and

a pull up load connected to the ready/busy pin.

13. (Previously presented) The semiconductor memory device of claim 12, wherein the memory device is in a busy state during a power-up period when the voltage at the ready/busy pin is at a low state.

14. (Previously presented) The semiconductor memory device of claim 13, wherein the memory device is in a ready state after the power-up period.

15. (Currently Amended) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a command register configured to generate a command busy signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal and the command busy signal; and

a ready/busy driver configured to drive a ready/busy signal in response ~~that is responsive~~ to the busy enable signal~~; and~~.

~~a command register coupled to an input of the ready/busy driver controller.~~

16. (Previously presented) The semiconductor memory device of claim 15, wherein the command register comprises:

a program command register configured to provide a program busy signal to the ready/busy driver controller; and

an erase command register configured to provide an erase busy signal to the ready/busy driver controller.

17. (Previously presented) The semiconductor memory device of claim 16, wherein the program busy signal indicates that the memory device is in a program mode.

18. (Previously presented) The semiconductor memory device of claim 16, wherein the erase busy signal indicates that the memory device is in an erase mode.

19. (Previously presented) A method of operating a semiconductor memory device, the semiconductor memory device including a voltage level detector, a ready/busy driver controller, a ready/busy driver, and a command register, the method comprising:

sensing a voltage with the voltage level detector;

generating a power-up signal with the voltage level detector when the voltage is less than a minimum voltage required to operate the semiconductor memory device; and

generating at least one busy signal with the command register, the at least one busy signal indicative of an operational state of the semiconductor memory device; and

generating a busy enable signal with the ready/busy driver controller in response to the power-up signal and the at least one busy signal.

20. (Previously presented) The method of operating a semiconductor memory device of claim 19, wherein generating a busy signal comprises generating a program busy signal.

21. (Previously presented) The method of operating a semiconductor memory device of claim 19, wherein generating a busy signal comprises generating an erase busy signal.

22. (Previously presented) The method of operating a semiconductor memory device of claim 19, further comprising generating a busy enable signal with the ready/busy driver controller, the busy enable signal generated when at least one chosen from the group consisting of the power-up signal and the busy signal is at a logic high state.

23. (New) A semiconductor memory device comprising:

a voltage level detector configured to sense a voltage and configured to generate a power-up signal while the voltage is less than a minimum voltage required to operate the device;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal, and including:

a control signal generator configured to generate a first and a second control signal in response to the power-up signal; and

a level shifter configured to generate the busy enable signal in response to the first and second control signals;

a ready/busy driver that is responsive to the busy enable signal; and

a command register coupled to an input of the ready/busy driver controller.

24. (New) A semiconductor memory device comprising:

a voltage level detector configured to sense a voltage and configured to generate a power-up signal while the voltage is less than a minimum voltage required to operate the device;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal;

a ready/busy driver that is responsive to the busy enable signal, and includes:

a ready/busy pin;

an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal; and

a pull up load connected to the ready/busy pin; and

a command register coupled to an input of the ready/busy driver controller.

25. (New) The semiconductor memory device of claim 24, wherein the memory device is in a busy state during a power-up period when the voltage at the ready/busy pin is at a low state.

26. (New) The semiconductor memory device of claim 25, wherein the memory device is in a ready state after the power-up period.